REMARKS

Claims 1-4 are all the claims pending in the application.

Claims 1-4 have been amended to address the Examiner's 35 U.S.C. 112 rejections. The amendments are not intended to narrow the scope of the claims.

Section 112, First Rejections

The Examiner rejects claims 1-4 as allegedly containing subject matter that was not described in the specification. Applicant traverses these rejections, because the claims, as amended are fully described in the specification. Specifically, regarding the limitation:

> logical operation information, wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal

this is fully supported by at least pages 5:24 to 8:9 and figures 1b, 1c, 3 and 5. Applicant also notes that in the Office Action, the Examiner states that the specification describes logical operation information and delay information for each path. Therefore, the Examiner is requested to withdraw the Section 112 first rejection.

Section 112, Second Rejections

The Examiner rejects claims 1-4 as allegedly containing subject matter that was not described in the specification. Applicant traverses these rejections, because the claims have been amended to address these rejections. Therefore, the Examiner is requested to withdraw the Section 112 second rejection.

Prior Art Rejections

The Examiner maintains the rejection of claims 1-4 as being unpatentable over *Blinne et al.* (U.S. Patent No. 5,274,568) in view of *Hasegawa* (U.S. Patent No. 6,041,168) (hereinafter *Hasegawa '168*) and in further view of *Hasegawa* (U.S. Patent No. 5,528,511) (hereinafter *Hasegawa '511*) under 35 U.S.C. § 103(a). Applicant traverses the rejection of claims 1-4 for at least the reasons discussed below.

Claims 1-4 are herein amended to more particularly require, wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal. The Examiner acknowledges that the combination of *Blinne* and *Hasegawa '168* fails to teach or suggest the claim element above (FOA pages 3-4). The Examiner asserts that Hasegawa '511 teaches this required claim element (FOA pages 4; Examiner *citing to Hasegawa '511* at Fig. 3; col. 1, lines 28-35; col. 2, lines 30-42; and col. 3, lines 5-26).

Hasegawa '511 at Fig 3 shows a timing diagram for two inputs and an output of an OR device (col. 4, lines 43-45; col. 1, lines 28 -35). As shown in Fig. 3, there is a 1ns delay from node p to node s due to interim device 230 (Figs. 2, 3, and 4). In contrast, node p to node v has no delay, 0 ns, because it is a short circuit. (Figs. 2, 3, and 4). Likewise transmission from node r to node s (path c) has no delay as this path is also a short circuit (Fig. 12). Also a transition, an R (rise) or an F (fall) is not a valid condition for path c, because it is a short circuit. Therefore, nodes r and s must be the same logic, hi or lo (col. 3, lines 17-27). At time equals 0 ns, the output terminal goes high as there is a difference in states at its input terminals, nodes s and v

(Fig. 3) and the output terminal goes high without delay. According to the timing diagram of Fig. 3 at time equals (from) 1 ns to 2 ns, the output terminal is high. However, this is counter-intuitive, given that no delay is taught for transmission from nodes s and v to node t, and that node s (path 250) rises to hi at 1 ns becoming the logic state equal to node v, the other input on an OR gate. Therefore, intuitively, one ordinarily skilled would expect the output terminal to fall to lo from 1 ns to 2 ns and then rise hi again as node v falls to lo.

Hasegawa '511 specifically teaches 0 ns delay for path f to g (col. 2, lines 34-35) and a 1 ns delay for path a to b to c to d (Figs 2, 3, and 4). Path d is the path from one input terminal of the OR gate to the output terminal of the same and path g is the other input to output path of the OR gate. This 1 ns delay is attributed to device 230 (col. 1, lines 20-23) and is not attributed to the OR gate or the path d.

Hasegawa '511 teaches delay time verifying, wherein rise and fall are not permitted between nodes connected by a short circuit (col. 3, lines 3-26). *Hasegawa '511* teaches 0 ns delay for path d and path g, the two input to one output paths of the OR gate. *Hasegawa '511* confusingly teaches an OR gate which fails to respond to two simultaneously hi inputs (Fig. 3). *Hasegawa '511* teaches that input to output paths in a given OR gate are equal with respect to delay. *Hasegawa '511* fails to teach delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as taught by the subject application and required by the claims (Fig. 5-7; claims 1-4). *Blinne*, *Hasegawa '168,* and *Hasegawa* '511, fail to teach or suggest, either alone or in combination, delay time information that is specific to an input terminal logical state transition and resulting logical state

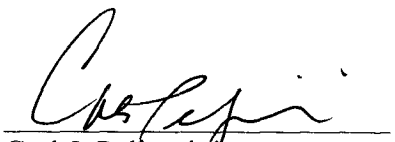
transition at an output terminal. At least for this deficiency, the rejection of claims 1-4 as being unpatentable over *Blinne* in view of *Hasegawa '168* and in further view of *Hasegawa '511* under 35 U.S.C. § 103(a), should be withdrawn.

Applicant notes that in the Office Action, in the Response to Arguments section, the Examiner appears to acknowledge the overall arguments. However, the Examiner repeats argument from the main body of the Office Action rather than specifically addressing Applicant's analysis as to why *Hasegawa '511* is deficient. The Examiner is requested to specifically address Applicant's analysis of *Hasegawa '511*.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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